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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,049	07/28/2003	Christoph Stefan Randazzo	DE03 0210	9286

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EXAMINER	
PRUCHNIC, STANLEY J	
ART UNIT	PAPER NUMBER
2859	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,049	RANDAZZO, CHRISTOPH STEFAN	
	Examiner	Art Unit	
	Stanley J. Pruchnic, Jr.	2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004 and 08 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 24 September 2004 have been fully considered but they are not persuasive.

2. In response to applicant's argument that the disclosure of EGERER *et al.* (U. S. Patent No. 6,744,304 B2, hereinafter **EGERER**) is directed to providing a time delay circuit: Applicant acknowledges that EGERER "relates to an electronic circuit for generating an output voltage having a defined temperature dependence." See "Remarks/Arguments", filed 24 September 2004, on Page 7. This is considered to be a temperature measurement function, as claimed by Applicant, providing an output voltage that depends on temperature. The intended use disclosed by EGERER is not considered relevant since EGERER discloses the output voltage V_A is temperature dependent (Col. 6, Lines a4-45), and thus is a "temperature measurement function", since this output could also be used for measurement of a temperature.

3. In response to applicant's argument that the combination of **EGERER** and BISPING *et al.* (U. S. Patent No. 6,726,361 B2, hereinafter **BISPING**) is not proper: Regarding their classification. A review of patents classified in 374/178 will show that many of them are cross-referenced in 327/512 and/or 327/513 because they include closely related subject matter. Further evidence suggesting that their respective disclosures include related subject matter, is provided by their respective listed fields of search. EGERER includes subclass 327/513, which is an indented subclass subordinate to 327/512, which is listed in the field of search for BISPING. Moreover, the invention claimed by Applicant is not limited to temperature measurement, but requires a search in Class 327 where electronic devices including functions related to temperature measurement may be found. PTAT circuits have wider application in the electronics art, for temperature measurement (374/178) and also for temperature compensation (327/513).

4. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, **EGERER** discloses all the limitations claimed except the feature taught by BISPING, which is very well known in the art. BISPING's teaching has not been shown to render EGERER's device to not function as intended by EGERER.

5. Regarding Applicant's argument against the rejection of Claim 7, it has not been shown how the teaching of MORRIS (U.S. Patent No. 4,305,288 A) is incompatible with the apparatus of EGERER in view of BISPING or Applicant's claimed invention. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Priority

6. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

7. The drawings were received on 24 September 2004. The Examiner APPROVES these drawings.

Claim Objections

8. Claim 16 is FINALLY objected to because of the following informalities: Claim 16 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the

claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 1 is already an "open-ended" claim by use of the word "comprising". The word "including" in Claim 16 also describes an "open-ended" claim 16. Claiming that another "open-ended" device includes the same apparatus fails to limit either the apparatus or the device since no additional elements are claimed.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

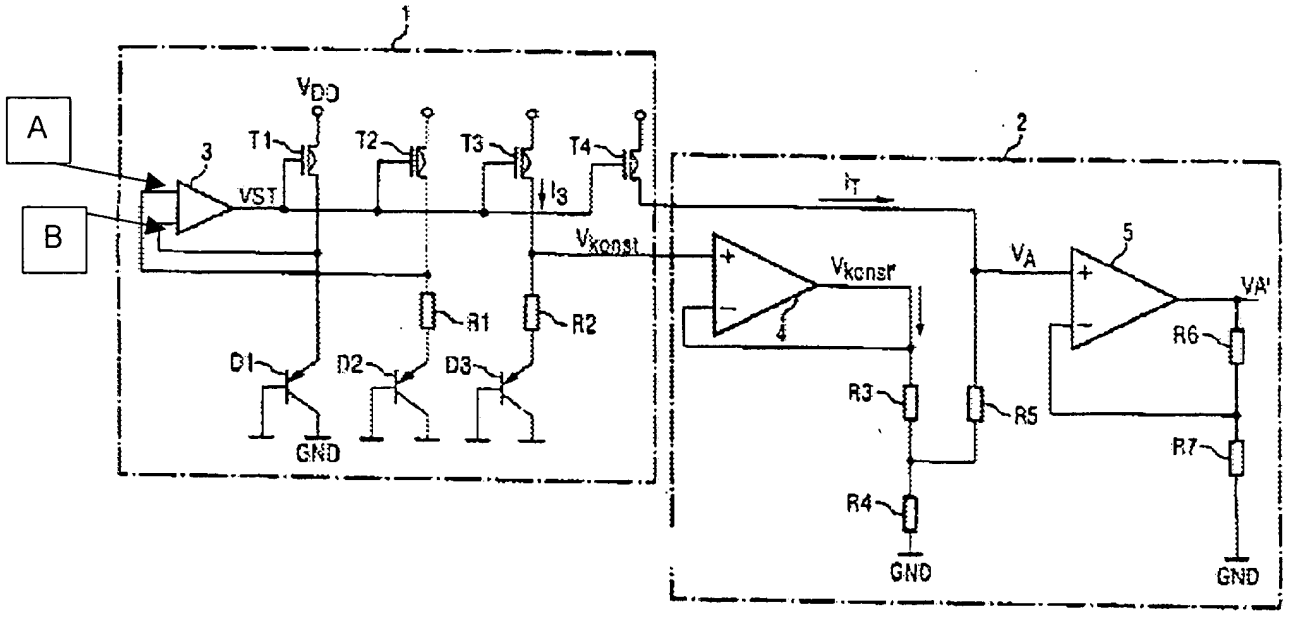
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. ***It is noted*** that the "output stage" claimed in Claim 1, Lines 14-18, lacks any claimed structural cooperative relationships with the remaining elements of the apparatus. Similarly, in Claims 14-15, the "temperature compensation network", *etc.*, lacks any claimed structural cooperative relationships with the remaining elements of the apparatus; and, in Claim 17, the "analog-to-digital converter", lacks any claimed structural cooperative relationships with the remaining elements of the claimed device or apparatus.

For consideration as to the merits, the omitted structural cooperative relationships are not considered essential to the claimed invention. See MPEP § 2172.01 wherein the following is stated: ">But see *Ex parte Nolden*, 149 USPQ 378, 380 (Bd. Pat. App. 1965) ("[I]t is not essential to a patentable combination that there be interdependency between the elements of the claimed device or that all the elements operate concurrently toward the desired result"); *Ex parte Huber*, 148 USPQ 447, 448-49 (Bd. Pat. App. 1965) (A claim does not necessarily fail to comply with 35 U.S.C. 112, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes.).<"

11. **Claims 1-4, 9, 10 and 12-18** are FINALLY rejected under 35 U.S.C. 103(a) as being unpatentable over EGERER *et al.* (U. S. Patent No. 6,744,304 B2, hereinafter **EGERER**) in view of BISPING *et al.* (U. S. Patent No. 6,726,361 B2, hereinafter **BISPING**).

EGERER discloses or suggests all the limitations as claimed by Applicant in Claims 1-4, 9, 10 and 12-18, including an apparatus 1 for performing a temperature measurement function, comprising a first stage with a first circuit (D2, T2; see the Figure, reproduced on next page) and a second circuit (D1, T1) being arranged in parallel, said first circuit comprising a first transistor (T2), a first resistor (R1), and a parallel arrangement of n diodes (D2), said second circuit comprising a second transistor (T1) and a parallel arrangement of m diodes (D1), an operational amplifier (3) on the input side being connected to the first circuit and the second circuit, said operational amplifier (3) applying a gate voltage to said first transistor (T2) and said second transistor (T1), said apparatus 1, further comprising an output stage (2) with p output transistors (T4), and an output resistor (R5) performing a current to output voltage conversion (VA) in order to provide an output voltage that depends on the actual temperature as claimed by Applicant in Claim 1.



EGERER further discloses first transistor (T2) provides a first current flowing through the parallel arrangement n diodes (D2) and said second transistor (T1) provides a second current flowing through the parallel arrangement of m diodes (D1) as claimed by Applicant in Claim 2.

EGERER further discloses said operational amplifier 3 has a first input (not labeled in EGERER, but annotated "A" in reproduced Figure, *above*), a second input (annotated "B" in reproduced Figure, *above*), and an output (VST), the first input (A) being connected to a drain of the first transistor (T2) and the second input (B) being connected to a drain of the second transistor (T1), said output (VST) being connected to a gate of said first transistor (T2) and a gate of said second transistor (T1) for biasing these transistors (T2, T1) as claimed by Applicant in Claim 3.

EGERER further discloses said output stage 2 amplifies said[sic] first current to obtain a third current (I_T) before performing said current to output voltage conversion by converting said third current (I_T) into said output voltage (A) as claimed by Applicant in Claim 4.

Regarding the limitation wherein the number n, m and p are integer numbers as claimed by Applicant in Claim 9: EGERER discloses each of these elements as a single device, *i.e.,* p output transistors, where p=1, and diodes where n=1 and m=1.

EGERER further discloses diode-connected PNP bipolar transistors serve as diodes (Col. 3, Lines 41-43 and Col. 5, Lines 24-33) as claimed by Applicant in Claim 10 and the output voltage and the actual temperature have a linear dependency (Col. 6, Lines 14-27 and Col. 4, Line 61- Col. 5, Line 21) as claimed by Applicant in Claim 12.

EGERER further discloses the gate voltage is applied to gates of the p output transistors (T4) as claimed by Applicant in Claim 13.

EGERER further discloses a temperature compensation network (comprising elements R2 and D3) providing a bandgap reference voltage (V_{KONST}) at another output as claimed by Applicant in Claim 14.

EGERER further discloses a device comprising the apparatus as claimed by Applicant in Claim 16 since he states the apparatus is intended to be used in combination with other devices/apparatus (*e.g.,* see Col. 1); and further regarding Claim 16, EGERER further discloses a device including the apparatus and an analog-to-digital converter 5 (in block 2 of the Figure), and regarding Claim 18, the analog-to-digital converter 5, for example, comprises an analog (input) and digital (output) device and so is a "mixed-mode" device, therefore the device of EGERER is part of such a device, since it includes such devices within its own bounds.

EGERER as described above, does not explicitly teach D1 is a parallel arrangement of n diodes and D2 is a parallel arrangement of m diodes as claimed by Applicant in Claim 1.

BISPING discloses that is known in the art to provide a parallel arrangement of "*x*" diodes with a predetermined surface area in order to provide a desired ratio of (effective) surface areas between two diodes (Col. 5, Lines 10-62) to provide a circuit that provides a voltage difference directly proportional to temperature (PTAT) in a simple and accurate manner (Col. 5, Lines 63-67).

BISPING is evidence that ordinary workers in the field of temperature measurement would recognize the benefit of using parallel arrangements of n and m

diodes as taught by BISPING for the diodes having a set ratio of emitter areas of EGERER in order to precisely choose the ratio of emitter areas of the diodes for providing a PTAT voltage output in a simple and accurate manner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute parallel arrangements of n and m diodes for the diodes having a set ratio of emitter areas of EGERER in order to precisely choose the ratio of emitter areas of the diodes for providing a PTAT voltage output in a simple and accurate manner as taught by BISPING.

Further regarding Claim 15: **EGERER** does not explicitly teach the temperature compensation network comprises a plurality of voltage followers with an implemented offset, the voltage followers being connected in series, as claimed by Applicant in Claim 15.

BISPING discloses that is known in the art to provide a temperature sensor with a compensation network comprising a plurality of voltage followers (OPV1, Fig. 2) for providing an internal reference voltage V_{ref} (Col. 9, Lines 30-67).

BISPING is evidence that ordinary workers in the field of temperature sensing would recognize the benefit of using a compensation network comprising a plurality of voltage followers as taught by BISPING for the temperature sensor of EGERER in order to extend the temperature range of the device.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute a compensation network comprising a plurality of voltage followers for the bandgap circuit of EGERER in order to extend the temperature range of the device as taught by BISPING.

12. **Claims 5, 6 and 8** are FINALLY rejected under 35 U.S.C. 103(a) as being unpatentable over **EGERER** in view of **BISPING** as applied to Claims 1-4, 9, 10 and 12-18 above, and further in view of **SAKURAI** (U.S. Patent No. 5,993,060 A).

EGERER discloses or suggests all the limitations as claimed by Applicant in Claims 5, 6 and 8 as described above in Paragraph 12 regarding Claims 1-4, 9, 10 and 12-18, including the limitations wherein the first resistor (R1) and output resistor (R5) are designed to minimize mismatch effects by using the same type of resistor in each case (Col. 6, Lines 45-51), in order to have the same intrinsic temperature dependence of resistance. **EGERER** does not explicitly teach said first transistor (T2) and said output transistors (T4) are designed to minimize mismatch effects or that the resistors R1 and R5 are both either integrated Npoly resistors or Ppoly resistors or that the output resistor is realized by a plurality of r resistors, the resistance of the output resistor (R5) being r times the resistance of said first resistor (R1), r being an integer number as claimed by Applicant.

SAKURAI discloses that is known in the art to provide resistors as integrated Npoly resistors or Ppoly resistors in order to minimize the temperature coefficient of resistance of the resistors (Col. 5, Lines 1-12). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Npoly resistors or Ppoly resistors for the resistors of **EGERER** in order to minimize the temperature coefficient of resistance of the resistors as taught by SAKURAI.

SAKURAI discloses that is known in the art to provide a resistor as provide a group of "***r***" resistors 3 (***r*** being an integer) in order to make adjustable the net resistance value of the group of resistors (Col. 4, Lines 52-63). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute a resistor array for the resistor of **EGERER** in order to make adjustable the net resistance value of the group of resistors (being R5) as taught by SAKURAI.

SAKURAI discloses that is known in the art to provide transistors of the same dimensions and electrical characteristics, designed to minimize mismatch effects (Col. 4, Lines 52-63). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide transistors of the same dimensions and electrical characteristics, to design the transistors to minimize mismatch effects as taught by SAKURAI.

13. **Claim 7** is FINALLY rejected under 35 U.S.C. 103(a) as being unpatentable over **EGERER** in view of **BISPING** as applied to Claims 1-4, 9, 10 and 12-18 above, and further in view of **MORRIS, JR.** (U.S. Patent No. 4,305,288 A, hereinafter MORRIS).

EGERER discloses or suggests all the limitations as claimed by Applicant in Claim 7 as described above in Paragraph 12 regarding Claims 1-4, 9, 10 and 12-18, but **EGERER** does not explicitly teach the limitation wherein the apparatus comprises a hold-capacitor being arranged in parallel to the output resistor (R5) as claimed by Applicant.

MORRIS discloses that is known in the art to provide a hold-capacitor with for filtering unwanted signals (Col. 1, Lines 58-68). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add a capacitor arranged in parallel to the output resistor in order to filter unwanted noise signals as taught by MORRIS.

14. **Claim 11** is FINALLY rejected under 35 U.S.C. 103(a) as being unpatentable over **EGERER** in view of **BISPING** as applied to Claims 1-4, 9, 10 and 12-18 above, and further in view of TUTHILL (U.S. Patent No. 5,982,221 A).

EGERER discloses or suggests all the limitations as claimed by Applicant in Claim 7 as described above in Paragraph 12 regarding Claims 1-4, 9, 10 and 12-18, but **EGERER** does not explicitly teach said operational amplifier (3) is a low-offset operational amplifier as claimed by Applicant in Claim 11.

TUTHILL discloses that is known in the art to provide a temperature sensor with a low-offset operational amplifier in order to benefit from more accurate measurements (Col. 3, Lines 38-61).

TUTHILL is evidence that ordinary workers in the field of temperature measurement would recognize the benefit of using a low-offset operational amplifier as taught by TUTHILL for the operational amplifier of EGERER in order to obtain more accurate measurements.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute a low-offset operational amplifier for the operational amplifier of EGERER in order to obtain more accurate measurement results as taught by TUTHILL.

Conclusion

15. **THIS ACTION IS** MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanley J. Pruchnic, Jr., whose telephone number is **(571) 272-2248**. The examiner can normally be reached on weekdays (Monday through Friday) from 7:30 AM to 4:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego F. F. Gutierrez can be reached at **(571) 272-2245**.

The ***Official FAX*** number for Technology Center 2800 is **(703) 872-9306** for ***all official communications***.

Any inquiry of a general nature or relating to the status of this application or proceeding may be directed to the official USPTO website at **http://www.uspto.gov/** or you may call the **USPTO Call Center** at **800-786-9199** or 703-308-4357. The Technology Center 2800 Customer Service FAX phone number is (703) 872-9317.

The cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources.

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SJP

Stanley J. Pruchnic, Jr.
2/23/05

G. Verbitsky

GAIL VERBITSKY
PRIMARY EXAMINER